High Speed Logic Isolator with Power Transformer

AD260

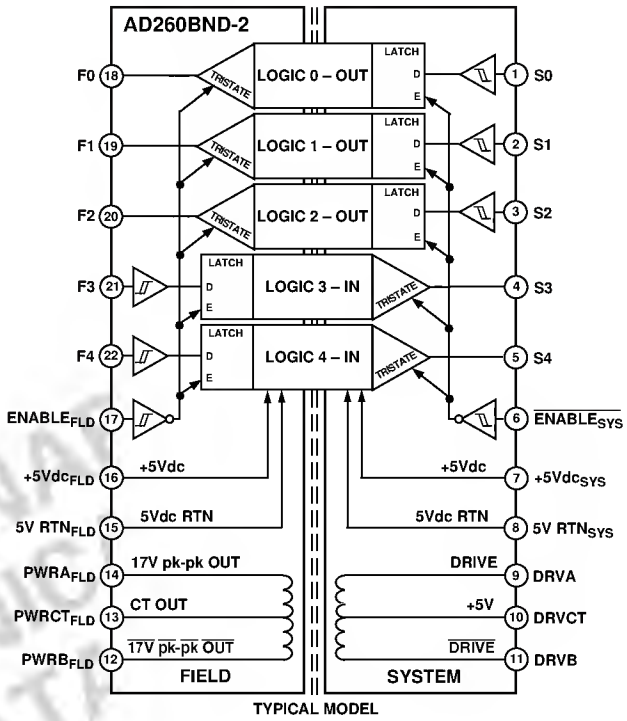
FEATURES

Isolation Voltage Rating: 4,000 V rms (Tested @ 6.4 kV rms)
Five Isolated Logic Lines: Available in Six I/O Configurations
Logic Signal Bandwidth: 20 MHz (min)
CMV Transient Immunity: 10 kV/μs
Waveform Edge Transmission Symmetry: ±1 ns
Isolated Power Transformer: 34 V p-p, 1.5 W max
Field and System Output Enable/Three-State Functions
Performance Rated Over –25°C to +85°C
Intrinsically Safe (CSA) and CE Certified for Application

APPLICATIONS

PLC/DCS Analog Input and Output Cards
Communications Bus Isolation
General Data Acquisition Applications
IGBT Motor Drive Controls
High Speed Digital I/O Ports

FUNCTIONAL BLOCK DIAGRAM



TYPICAL MODEL

GENERAL DESCRIPTION

The AD260 is designed to isolate five digital control signals to/from a microcontroller and its related field I/O components. Six models allow all I/O combinations from five input lines to five output lines, including combinations in between. Every AD260 effectively replaces up to 5 optos while also providing the 1.5 W transformer for a 4 kV dc-dc power supply circuit.

Each line of the AD260 has a bandwidth of 20 MHz (min.) with a propagation delay of only 11 ns, which allows for extremely fast data transmission. Output waveform symmetry is maintained to within ±2 ns of the input so the AD260 can be used to accurately isolate time-based PWM signals.

All field or system output pins of the AD260 can be set to a three-state level by use of the two enable pins. A field output three-stated offers a convenient method of presetting logic levels at power-up by use of pull-up/down resistors. System outputs three-stated allow easy multiplexing of multiple AD260s.

The isolation barrier of the AD260 is rated at 4 kV rms (system to field) and 100% tested to 6,400 V rms. The barrier design also provides excellent transient immunity from 10 kV/μs common-mode voltage excursions of field terminals with no false output triggering.

Each output is updated by input logic transitions, the AD260 also has a continuous output update feature that automatically updates each output. This guarantees the output is always valid 10 μs after power-up or fault conditions.

The AD260 also has an integral center tap transformer for generating isolated power. Typically driven by a 5 V push-pull drive at the primary, it will generate a 34 V p-p output capable of supplying up to 1.5 W. This can then be regulated to the desired voltage, including ±5 V dc for circuit components and 24 V for a 20 mA loop supply when needed.

PRODUCT HIGHLIGHTS

Five Isolated Logic Line I/O Configurations Available: The AD260 is available in six pin compatible versions of I/O configurations to meet a wide variety of requirements.

Wide Bandwidth with Minimal Edge Error: The AD260 affords extremely fast isolation of logic signals due to its 20 MHz bandwidth while maintaining a waveform input-to-output edge transition error of less than ±2 ns (total).

4,000 V rms Working Voltage Isolation Rating: The AD260 is rated to operate at 4,000 V rms (signal and power) and is 100% production tested at 6,400 V rms, using a "VDE-0884" test method.

High Transient Immunity: The AD260 rejects common-mode transients varying at up to 10 kV/μs without false triggering or damage to the device.

(*Continued on page* 6)

REV. 0

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AD260–SPECIFICATIONS (Typical at T_A = +25°C, +5 V dc_{SYS}, + 5 V dc_{FLD}, T_{RR} = 50 ns min unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS					
Threshold Voltage					
Positive Transition (V_{T+})	+5 V dc_{SYS} = 4.5 V	2.0	2.7	3.15	V
	+5 V dc_{SYS} = 5.5 V	3.0	3.2	4.2	V
Negative Transition (V_{T-})	+5 V dc_{SYS} = 4.5 V	0.9	1.8	2.2	V
	+5 V dc_{SYS} = 5.5 V	1.2	2.2	3.0	V
Hysteresis Voltage (V_H)	+5 V dc_{SYS} = 4.5 V	0.4	0.9	1.4	V
	+5 V dc_{SYS} = 5.5 V	0.5	1.0	1.5	V
Input Capacitance (C_{IN})			5		pF
Input Bias Current (I_{IN})	Per Input		10		pA
OUTPUT CHARACTERISTICS					
Output Voltage[1]					
High Level (V_{OH})	+5 V dc_{SYS} = 4.5 V, $\|I_O\|$ = 0.02 mA	4.4			V
	+5 V dc_{SYS} = 4.5 V, $\|I_O\|$ = 4 mA	3.7			V
Low Level (V_{OL})	+5 V dc_{SYS} = 4.5 V, $\|I_O\|$ = 0.02 mA			0.1	V
	+5 V dc_{SYS} = 4.5 V, $\|I_O\|$ = 4 mA			0.4	V
Output Three-State Leakage Current	$ENABLE_{SYS/FLD}$ @ Logic Low/High Level Resp.		0.5		µA
DYNAMIC RESPONSE					
Max Logic Signal Frequency (f_{MIN})	50% Duty Cycle, +5 V dc_{SYS} = 5 V	20			MHz
Waveform Edge Symmetry Error (t_{ERROR})	t_{PHL} vs. t_{PLH}		±1		ns
Logic Edge Propagation Delay (t_{PHL}, t_{PLH})			14	20	ns
Minimum Pulse Width (t_{PWMIN})		25			ns
Max Output Update Delay on Fault/Pwr Up				12	µs
ISOLATION BARRIER RATING					
Operating Isolation Voltage (V_{CMV})	100% Tested, 60 Hz AC Sinusoidal	4,000			V rms
Isolation Rating Test Voltage ($V_{CMV\,TEST}$)	Method VDE-0884, IEC-804.x	6,400			V rms
Transient Immunity ($V_{TRANSIENT}$)			10,000		V/µs
Isolation Mode Capacitance (C_{ISO})	Total Capacitance, All Lines & Transformer		10	15	pF
Capacitive Leakage Current (I_{LEAD})	240 V rms @ 60 Hz			2	µA rms
POWER TRANSFORMER					
Primary Winding	Bifilar Wound, Center-Tapped				
Inductance (L_P)	Each Half		1		mH
Number of Turns (N_P)	Each Half		26		Turns
Max Volt-Seconds (E × t)	Each Half			27	V × µs
Recommended Operating Frequency	–25°C to +85°C, Push-Pull Drive	150	200	250	kHz
Absolute Min Operating Frequency	–25°C to +85°C, Push-Pull Drive	65			kHz
Secondary Winding	Bifilar Wound, Center-Tapped				
Number of Turns (N_S)	Each Half		48		Turns
Insulation Withstand	Primary to Secondary	4,000	V rms		
Capacitance	Primary to Secondary		5		pF
Recommended Max Power	Rated Performance		1.5		W
POWER SUPPLY					
Supply Voltage (+5 V dc_{SYS} & 5 V dc_{FLD})	Rated Performance	4.75		5.5	V dc
	Operating	4.0		5.5	V dc
Power Dissipation Capacitance (C_{PD})	Effective, Per Channel, Each Side		20		pF/Channel
Current (I_{SYS}, I_{FLD})[2]	Quiescent, Each Side		3.5		mA
Current (I_{SYS}, I_{FLD})[2]	All Lines at 10 MHz, Each Side		13.5		mA
TEMPERATURE RANGE					
Rated Performance (T_A)		–25		+85	°C
Storage (T_{STG})		–25		+85	°C

NOTES

[1]Output state is determined by input edge transition direction, as is typical for a standard SET/RESET Flip-Flop.

[2]Excludes power for transformer system side drive or field side regulation circuitry.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

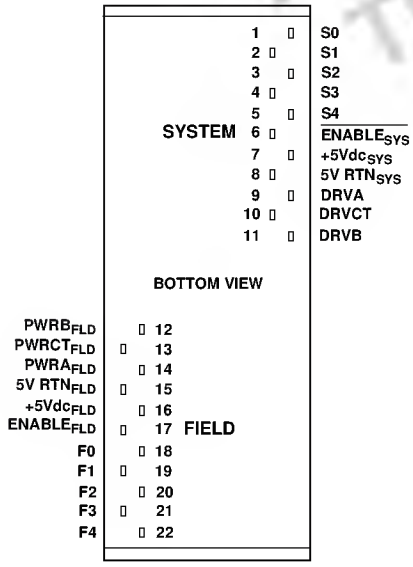
Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage (+5 V $dc_{SYS\ \&\ FLD}$)		–0.5		+6.0	V
DC Input Voltage ($V_{IN\ MAX}$)	Referred to +5 $Vdc_{SYS\ \&\ FLD}$ and 5 V $RTN_{SYS\ \&\ FLD}$ Resp.	–0.5		+0.5	V
DC Output Voltage ($V_{OUT\ MAX}$)	Referred to +5 V $RTN_{SYS\ \&\ FLD}$ and 5 V $DC_{SYS\ \&\ FLD}$ Resp.	–0.5		+0.5	V
Clamp Diode Input Current (I_{IK})	for V_I < –0.5 V or V_I > 5 V $RTN_{SYS\ \&\ FLD}$ +0.5 V	–25		+25	mA
Clamp Diode Output Current (I_{OK})	for V_O < –0.5 V or V_O > 5 V $RTN_{SYS\ \&\ FLD}$ +0.5 V	–25		+25	mA
Output DC Current, per pin (I_{OUT})		–25		+25	mA
DC Current, V_{CC} or GND (I_{CC} or I_{GND})		–50		+50	mA
Storage Temperature (T_{STG})		–65		+125	°C
Lead Temperature (Soldering, 10 s)				+300	°C
Electrostatic Protection (V_{ESD})	per MIL-STD-883, Method 3015	2			kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model Number	Description	Package Description	Package Option
AD260BND-0	0 Input, 5 Output Lines	Plastic DIP	ND-22
AD260BND-1	1 Input, 4 Output Lines	Plastic DIP	ND-22
AD260BND-2	2 Input, 3 Output Lines	Plastic DIP	ND-22
AD260BND-3	3 Input, 2 Output Lines	Plastic DIP	ND-22
AD260BND-4	4 Input, 1 Output Lines	Plastic DIP	ND-22
AD260BND-5	5 Input, 0 Output Lines	Plastic DIP	ND-22

PINOUT



I/O CONFIGURATIONS AVAILABLE

The AD260 is available in several configurations each having the same 3 kV rms transformer. The choice of model is determined by the desired umber of input vs. output lines. All models have identical footprints with the power and enable pins always being in the same location.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1–5	S0 thru S4	Digital Xmt or Rev from F0 thru F4
6	$\overline{ENABLE}_{SYS}$	System Output Enable/Three-State
7	+5 V dc_{SYS}	System Power Supply (+5 V dc Input)
8	5 V RTN_{SYS}	System Power Supply Common
9	DRVA	Power Transformer Hi Drive
10	DRVCT	Power Transformer Center Tap (+5 V)
11	DRVB	Power Transformer Low Drive
12	$PWRB_{FLD}$	17 V p-p Sq. Wave Isolated Power
13	$PWRCT_{FLD}$	Isolated Power Xfrmr Center Tap
14	$PWRA_{FLD}$	17 V p-p Sq. Wave Isolated Power
15	5 V RTN_{FLD}	Field Power Supply Common
16	+5 V dc_{FLD}	Field Power Supply (+5 V Input)
17	$ENABLE_{FLD}$	Field Output Enable/Three-State
18–22*	F0 thru F4	Digital Xmt or Rcv from S0 thru S4

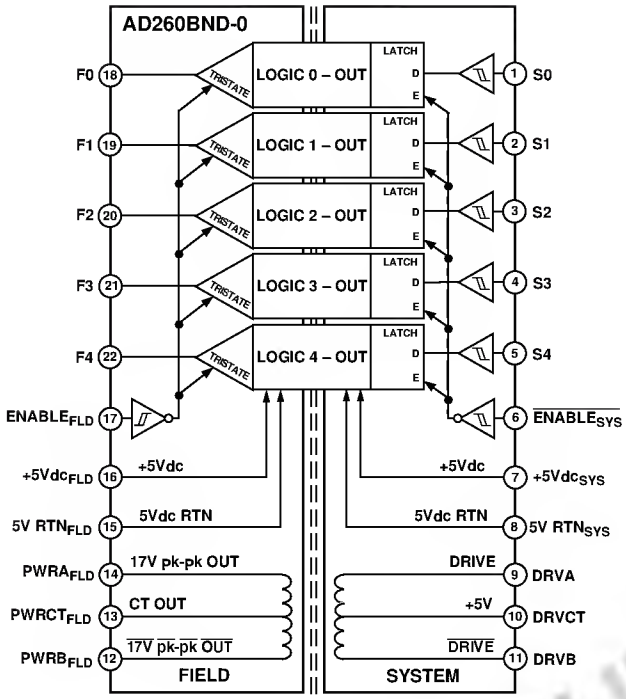
*Function of pin determined by model. Refer to Table I.

CAUTION

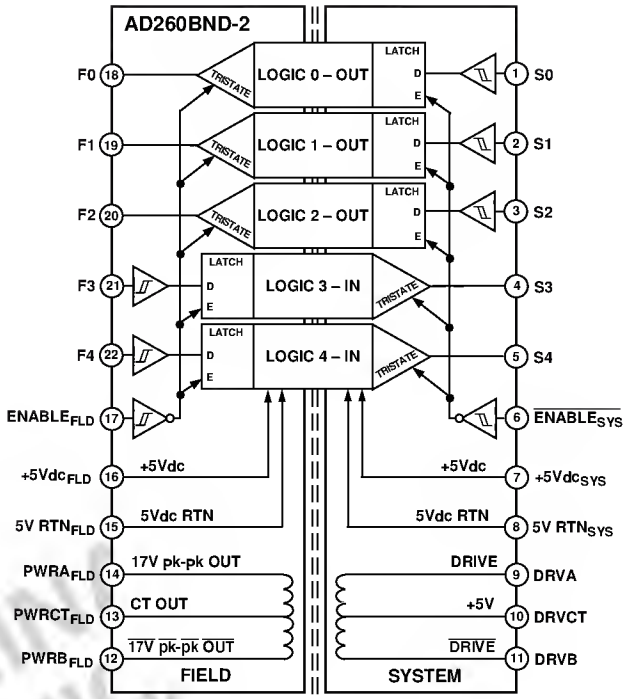
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD260 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

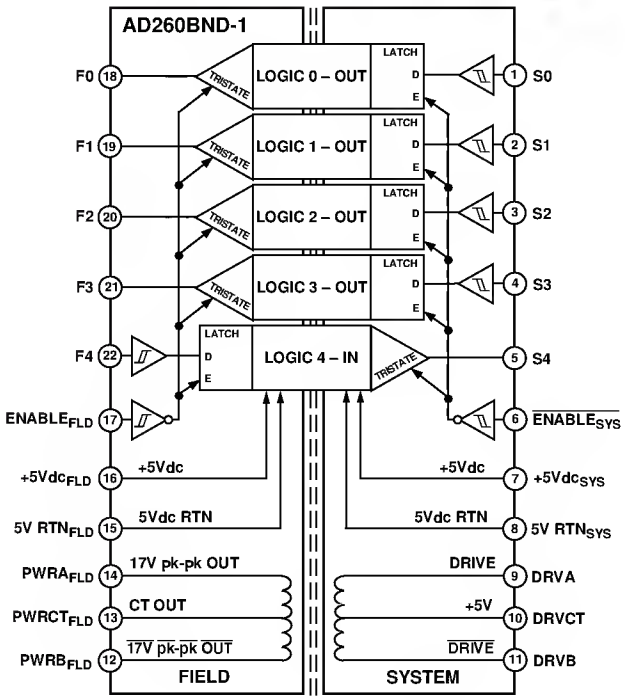
AD260BND-0



AD260BND-2



AD260BND-1



AD260BND-3

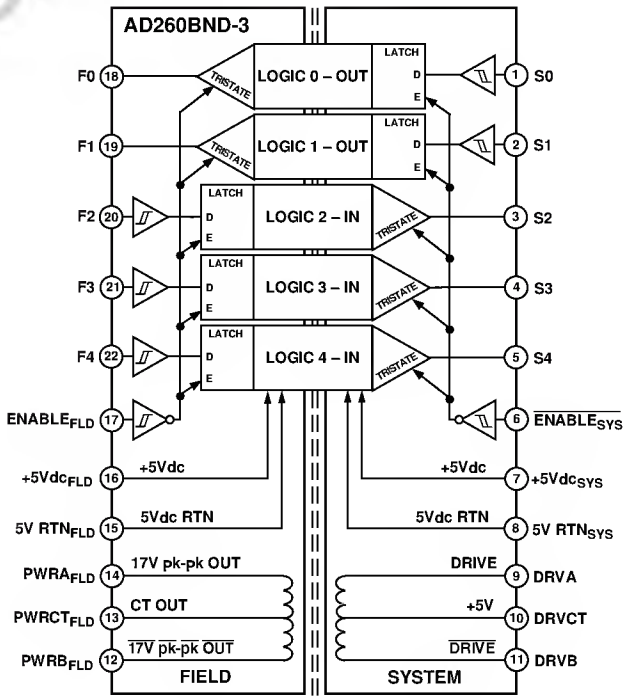
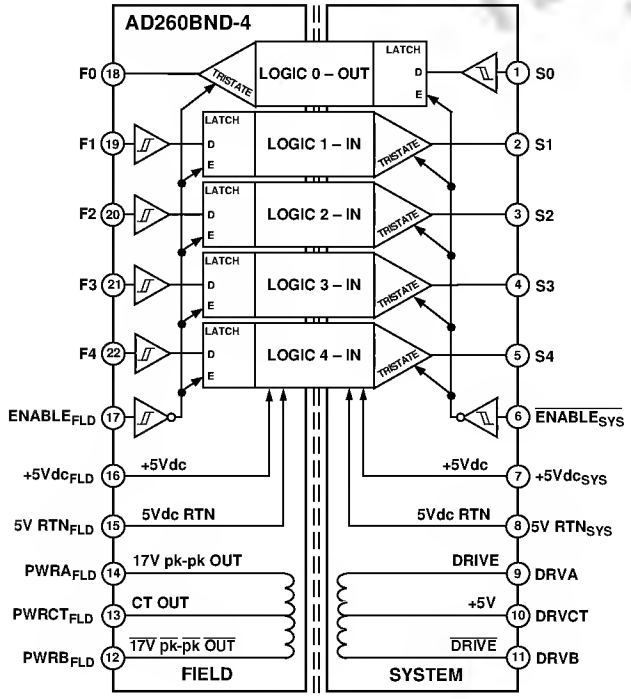


Table I.

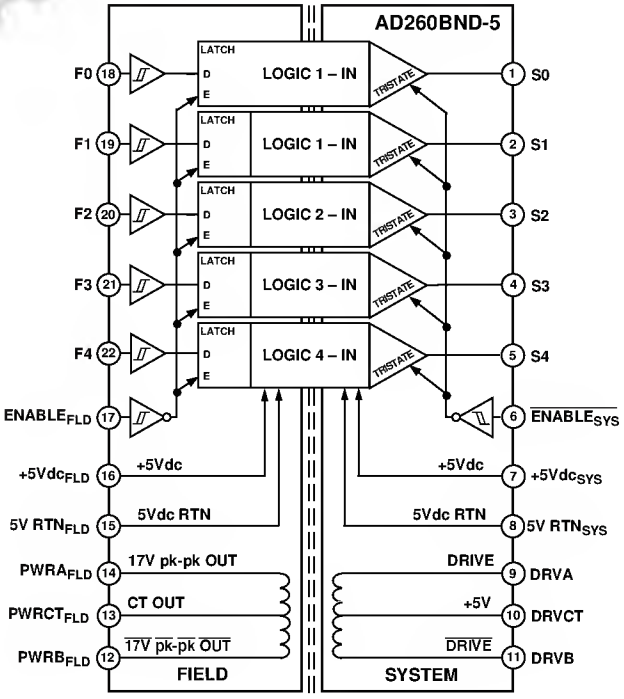
Pin	AD260BND-0	AD260BND-1	AD260BND-2	AD260BND-3	AD260BND-4	AD260BND-5
1	S0 (Xmt)	S0 (Xmt)	S0 (Xmt)	S0 (Xmt)	S0 (Xmt)	S0 (Rcv)
2	S1 (Xmt)	S1 (Xmt)	S1 (Xmt)	S1 (Xmt)	S1 (Rcv)	S1 (Rcv)
3	S2 (Xmt)	S2 (Xmt)	S2 (Xmt)	S2 (Rcv)	S2 (Rcv)	S2 (Rcv)
4	S3 (Xmt)	S3 (Xmt)	S3 (Rcv)	S3 (Rcv)	S3 (Rcv)	S3 (Rev)
5	S4 (Xmt)	S4 (Rev)	S4 (Rcv)	S4 (Rcv)	S4 (Rcv)	S4 (Rcv)
6	$\overline{\text{ENABLE}}_{\text{SYS}}$	*	*	*	*	*
7	+5 V dc_{SYS}	*	*	*	*	*
8	5 V RTN_{SYS}	*	*	*	*	*
9	DRVA	*	*	*	*	*
10	DRVCT	*	*	*	*	*
11	DRVB	*	*	*	*	*
12	PWRB	*	*	*	*	*
13	PWRCT	*	*	*	*	*
14	PWRA	*	*	*	*	*
15	5 V Rtn_{FLD}	*	*	*	*	*
16	+ 5 V dc_{FLD}	*	*	*	*	*
17	$\text{ENABLE}_{\text{FLD}}$	*	*	*	*	*
18	F0 (Rcv)	F0 (Rcv)	F0 (Rcv)	F0 (Rcv)	F0 (Rcv)	F0 (Xmt)
19	Fl (Rcv)	F1 (Rcv)	F1 (Rcv)	F1 (Rcv)	F1 (Xmt)	F1 (Xmt)
20	F2 (Rcv)	F2 (Rcv)	F2 (Rcv)	F2 (Xmt)	F2 (Xmt)	F2 (Xmt)
21	F3 (Rcv)	F3 (Rcv)	F3 (Xmt)	F3 (Xmt)	F3 (Xmt)	F3 (Xmt)
22	F4 (Rcv)	F4 (Xmt)	F4 (Xmt)	F4 (Xmt)	F4 (Xmt)	F4 (Xmt)

*Pin function is the same on all models, as shown in the AD260BND-0 column.

AD260BND-4



AD260BND-5



(*Continued from page* 1)

Field and System Enable Functions: Both the isolated and nonisolated sides of the AD260 have ENABLE pins that three-state all outputs. Upon reenabling these pins, all outputs are updated to reflect the current input logic level.

CE Certifiable: Simply by adding the external components shown in Figure 2, the AD260 can attain CE certification in most applications.

GENERAL ATTRIBUTES

The AD260 provides five HCMOS compatible isolated logic lines and a power isolation transformer.

Both the logic and power isolation circuits are tested for continuous 3 kV withstand operation.

>10 kV/μs common-mode transient immunity

The case design and terminal arrangement provides greater than 10 mm spacing between field and system side conductors, providing CSA/IS compatibility (see Figure 1).

The five unidirectional logic lines have six possible combinations of "ins" and "outs", or transmitter/receiver pairs; hence there are six AD260BND-n parts (see Table I).

Each 20 MHz logic line[1] has a Schmitt trigger input and a three-state output (on the other side of the isolation barrier) and 11 ns of propagation delay. A single enable pin on either side of the barrier causes all outputs on that side to go three-state and all inputs (driven pins) to ignore their inputs and retain their last known state.[2]

Edge "fidelity," or the difference in propagation time for rising and falling edges, is less than 1 ns.

Power consumption, unlike opto-isolators, is a function of operating frequency. Each logic line barrier driver requires about 130 μA per MHz and each receiver, 62 μA per MHz.

The total capacitance spanning the isolation barrier is less than 10 pF.

The power transformer is designed to operate between 150 kHz and 250 kHz and will easily deliver more than 1 W of isolated power (34 V center-tapped) when driven push-pull (5 V) on the system side. Different transformer tap, rectifier and regulator schemes will provide combinations of ±5 V, 15 V, 24 V or even 30 V or higher.

NOTES

[1] The minimum period of a pulse that can be accurately coupled across the barrier is about 25 ns. Therefore the maximum square-wave frequency of operation is 20 MHz.

[2] Logic information is sent across the barrier as "set-hi/set-lo" data that is derived from logic level transitions of the input. At power-up or after a fault condition, an output might not represent the state of the respective channel input to the isolator. An internal circuit operates in the background which interrogates all inputs about every 5 μs and sends appropriate "set-hi" or "set-lo" data across the barrier.
Recovery time from a fault condition or at power-up is normally between 5 μs to 10 μs.

Application Examples

High Side Current Driver

Digital Output Control of Solid State Relays and Motors

Level Sensing on a 4 to 20 mA Signal Line

RS-422/RS-485 Communications Bus Isolation

Power Supply Regulation and Monitoring

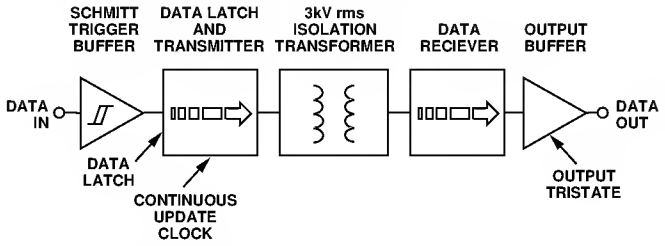


Figure 1. AD260 Simplified Block Diagram

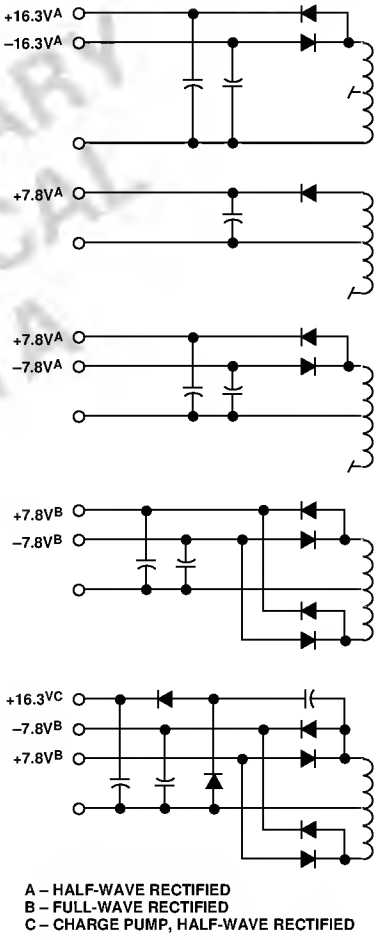


Figure 2. Isolated Power Transformer Rectification Examples

Application Examples

The following is an example of a typical transformer system-side drive circuit and a field-side regulation circuit suitable for use in most general applications.

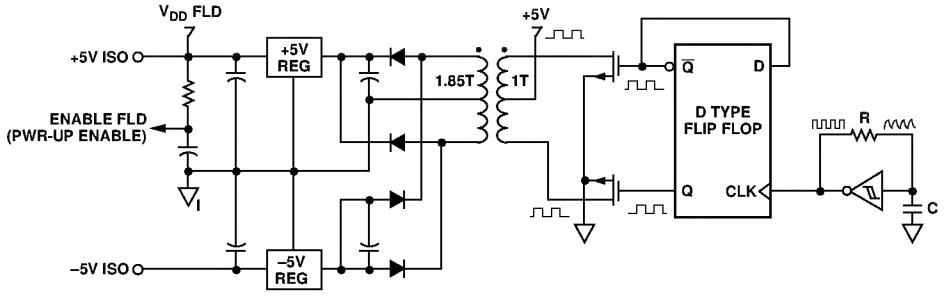
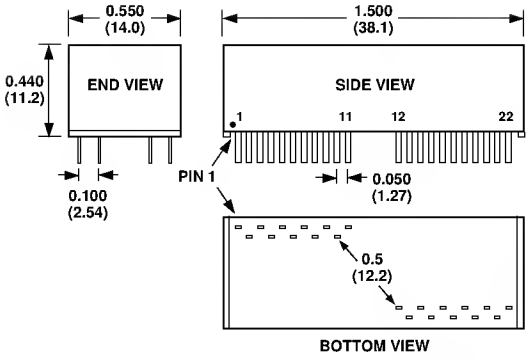


Figure 3.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

22-Pin Plastic DIP
(ND-22)



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